SUBMISSIONS

Claims 43, 50, 52, 54, 56, and 109-128 of the subject application are currently pending, and have been rejected by the Examiner in the Final Office Action mailed July 26, 2004. In the accompanying amendment, claims 43, 50, 52, 54, 56, 119, 122, 123, and 126 have been amended. Support for the amendments to the claims may be found in the written description, claims, and drawings of the subject application as originally filed. On account of the foregoing listed support for the amendments to the claims, it is respectfully submitted that the amendments do not add new matter.

Claim Rejections Under 35 U.S.C. § 112

The Examiner rejected claims 50, 52, 54, 56, and 109-128 under 35 U.S.C. § 112, second paragraph, because these claims contain the trademark terms "Java", which the Examiner asserts renders the scope of the claims unclear. In response, the Applicant has amended the claims to remove the term "Java" therefrom. Accordingly, the Examiner is respectfully requested to withdraw her rejection of claims 50, 52, 54, and 56, and 109-128 under 35 U.S.C. § 112, second paragraph.

Double Patenting

The Examiner has rejected claims 43, 50, 52, 54, 56, and 109-128 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-70 of U.S. Patent 6,332,215. In response, Applicant is filing simultaneously herewith, a terminal disclaimer in which a terminal portion of the claims of the subject application that extends beyond the term of the claims of the U.S. Patent 6,332,215, if the subject application were to mature into a granted patent is disclaimed. It is respectfully submitted that in view of the terminal disclaimer, the Examiner should withdraw her rejection of claims 43, 50, 52, 54, 56, and 109-128 under the judicially created doctrine of obviousness-type double patenting.

Claim Rejections Under 35 U.S.C. § 103

Claim 43 includes the following limitations:

A system comprising a central processing unit (CPU) core;
a register file associated with the CPU core; a hardware accelerator to process stack-based instructions in cooperation with the CPU core,

wherein the hardware accelerator marks variables associated with the
stack-based instructions in the register file as modified when the variables
are updated as a result of the processing of the stack-based instructions
to enable selective writing of the variables marked as modified to a
memory.
(Emphasis added)

For convenience, the Examiner's arguments regarding claim 43 are repeated

below:

> Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over
> Dickol et, al US 5,875,336 and further in view of Krall et al, the article XP-
> 002117590, Title: CACAO- a 64 bit JAVA VM just-in-time compiler,
> Source: Concurrency: Practice and Experience, vol 9 (11), page 1017-
> 1030, November, 1997.
>
> As per claim 43, Dickol discloses:
> -a central processing unit core (Abstract, Fig 2, Fig 3, col 4 lines 55-60) a
> register file associated with...memory (Abstract, col 3 lines 20-35, codes
> (col 3 lines 40-50, col 4 lines 10-15, col 4 lines 43-50).
>
> Dickol does not specifically disclose that the hardware processor is an
> accelerator. However, in the article Krall discloses that the processor is an
> accelerator (Krall, page 1017, summary and introduction). Therefore, it
> would have been obvious to one of the ordinary skill in the art at the time
> of invention was made to incorporate the teaching of Krall into the method
> of Dickol for introducing an accelerator. The modification would be
> obvious because one of the ordinary skill in the art would be motivated to
> compile, execute and run the programs faster than the regular hardware
> processor.
>
> Neither Dickol nor Krall disclose multiplexer. However, official notice is
> taken for multiplexer. The modification would be obvious because one of
> the ordinary skill in the art would be motivated to attach many
> communications lines to a smaller number of communications port
> efficiently.
> (Page 3-4, Office Action mailed July 27, 2004)

The Applicant has studied the pertinent portions of Dickol as indicated by the

Examiner i.e. (Abstract, col 3, lines 20-35, col 3, lines 40-50, col 4, lines 10-15, and col

4, lines 43-50), but finds no support for the Examiner's assertion that Dickol teaches the

above emphasized limitation of claim 43. In this regard, the Examiner is reminded that

the Examiner bears the burden of establishing a prima facie case of obviousness, and

the Applicant respectfully submits that the Examiner has failed to discharge this burden.

Accordingly, it is respectfully submitted that claim 43 is not obvious in view of the combination of Dickol and Krall.

With regard to claim 50. the Examiner argues as follows:

Neither Dickol nor Krall disclose generating new JAVA program counter. However, Tremblay disclose generating new JAVA program counter. (Tremblay, col 3, lines 40-50). The modification would be obvious because one of the ordinary skill in the art would be motivated to locate the address of the instruction to be executed efficiently.
(Page 5, Office Action mailed July 27, 2004)

In response to the above argument, the Applicant respectfully points out to the Examiner that claim 50 includes the following limitation:

"a hardware accelerator to process stack-based instructions in cooperation with the CPU core, wherein the hardware accelerator generates a new virtual machine program counter <u>due to a "GOTO" or "GOTO W" byte code by sign extending the immediate branch offset following the "GOTO" or "GOTO W" byte code and adds it to the virtual machine program counter of the current byte code instruction"</u>.
(Emphasis Added)

In the above argument, the Examiner is discussing the limitation of "generating a new Java program counter", which, with respect, is only part of the above limitation of claim 50 and ignores the emphasized portion. In other words, the Examiner has failed to show that the combination of Dickol and Krall teaches the above claim limitation <u>in its entirety</u>. Accordingly, claim 50 cannot be rendered obvious by the combination of Dickol and Krall as suggested by the Examiner.

With regard to claim 52, likewise, the Examiner in her argument, only discusses generating a new Java program counter, whereas the actual claim limitation of claim 52 recites:

"a hardware accelerator to process stack-based instructions in cooperation with the CPU core, wherein the hardware accelerator generates a new virtual machine program counter <u>due to a "JSR" or "JSR W" byte code by sign extending the immediate branch offset following the "JSR" or "JSR W" byte code and adding it to the virtual machine PC of the current byte code instruction, computes the return Virtual machine program counter and pushes the return Virtual machine program counter onto an operand stack as amended"</u>.
(Emphasis Added)

Thus, the Examiner has failed to show the combination of Dickol and Krall teaches the above limitation of claim 52 in its entirety including the emphasized portions. Accordingly, it is respectfully submitted that the combination of Dickol and Krall does not render claim 52 obvious.

In a similar vein, claim 54 includes the limitation of:

"a hardware accelerator to process stack-based instructions in cooperation with the CPU core; wherein the hardware accelerator <u>performs sign extension for the virtual machine SiPush and BiPush byte codes and appends the sign extended data to the immediate field of a register-based instruction being composed based the stack-based instructions</u>,"
(Emphasis Added)

And claim 56 includes the limitation of:

"a hardware accelerator to process stack-based instructions in cooperation with the CPU core, wherein the hardware accelerator <u>performs sign extension for the virtual machine SiPush and BiPush byte codes and makes the sign extended data available to be read by the CPU core</u>".
(Emphasis Added)

However, the Examiner in discussing only the limitation of generating a new Java program counter has failed to show that the combination of Dickol and Krall teaches the above quoted limitations of claims 54 and 56, respectively. Thus, it is respectfully submitted that the combination of Dickol and Krall does not render claim 54 or claim 56 obvious.

In arguing that claim 119 is obvious in view of the combination of Dickol and Krall, the Examiner simply states:

For claims 112-128, (Dickol, Abstract, col 6 lines 1-20, col 5, lines 1-25, col 4, lines 30-50, col 3 lines 40-50, col 4 lines 10-15, col 4 lines 43-50, Krall, page 1017).
(Page 6, Office Action Mailed July 27, 2004)

Claim 119 includes the following limitations:

a hardware accelerator to process stack-based instructions in cooperation with the CPU core, <u>wherein the hardware accelerator maintains an operand stack for the stack-based instructions in the register file such that the operand stack in the register file define a ring buffer in conjunction with an overflow/underflow mechanism for moving operands in the</u>

<u>operand stack between the register file and memory, and loads variables</u>
<u>required for processing the stack-based instructions into the register file.</u>
(Claim 119, emphasis added)

The Applicant has studied the above-identified portions of Dickol and Krall, but does not find any description of the above-emphasized limitation of claim 119. Once again, the Applicant asserts that the Examiner bears the initial burden of establishing a prima facie case of obviousness. It is respectfully submitted that the Examiner has failed to discharge this burden, and unless such a prima facie case is established, a rejection under 35 U.S.C. §103 is not proper. Accordingly, the Examiner is respectfully requested to withdraw her rejection of claim 119.

Each of the remaining claims is dependent on the one of the above-discussed independent claims, and accordingly it is respectfully submitted that the remaining dependent claims are also not obvious in view of the combination of Dickol and Krall.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Vani Moodley at (408) 720-8300.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: ____10/26/____2004

Vani Moodley
Under 37 CFR § 10.9(b)

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